

IR4426/IR4427/IR4428(S)&(PbF)

DUAL LOW SIDE DRIVER

Features

- Gate drive supply range from 6 to 20V
- CMOS Schmitt-triggered inputs
- Matched propagation delay for both channels
- Outputs out of phase with inputs (IR4426)
- Outputs in phase with inputs (IR4427)
- OutputA out of phase with inputA and OutputB in phase with inputB (IR4428)
- Also available LEAD-FREE

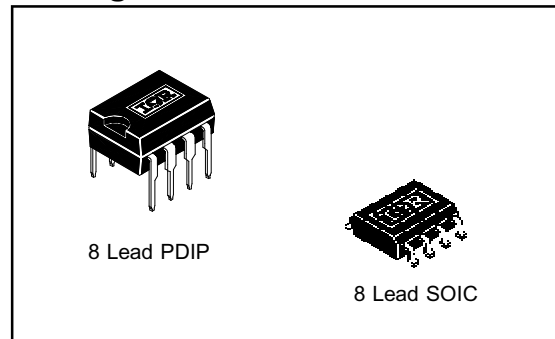
Descriptions

The IR4426/IR4427/IR4428 (S) is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

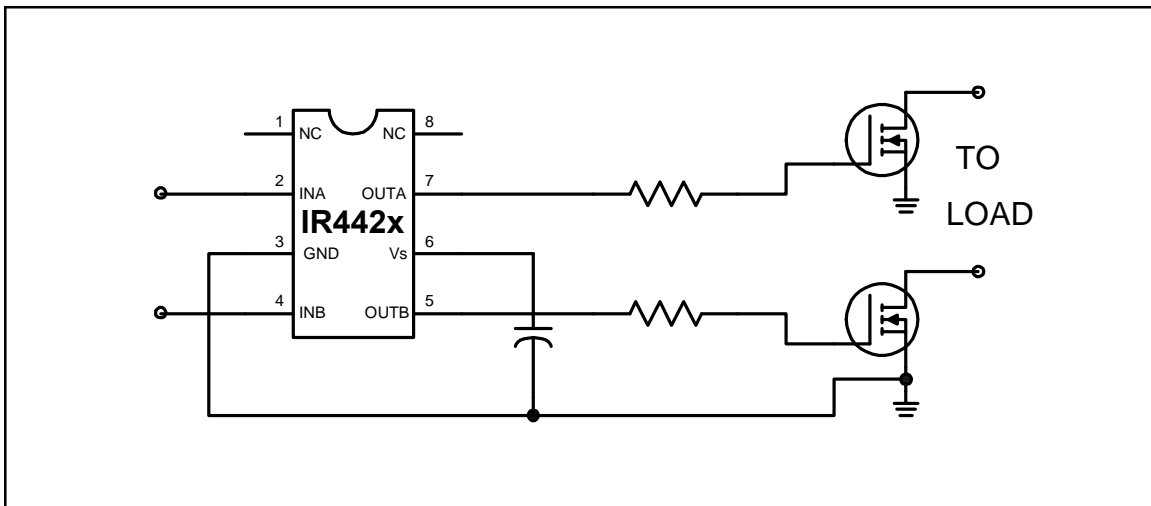
Product Summary

$I_{O+/-}$	1.5A / 1.5A
V_{OUT}	6V - 20V
$t_{on/off}$ (typ.)	85 & 65 ns

Packages



Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _S	Fixed supply voltage	-0.3	25	V	
V _O	Output voltage	-0.3	V _S + 0.3		
V _{IN}	Logic input voltage	-0.3	V _S + 0.3		
P _D	Package power dissipation @ T _A ≤ +25°C	(8 Lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R _{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND.

Symbol	Definition	Min.	Max.	Units
V _S	Fixed supply voltage	6	20	V
V _O	Output voltage	0	V _S	
V _{IN}	Logic input voltage	0	V _S	
T _A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{BIAS} (V_S) = 15V, T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V _{IH}	Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4426)	2.7	—	—	V	
	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4427)					
	Logic "0" input voltage (OUTA=LO), Logic "1" input voltage (OUTB=HI) (IR4428)					

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DC Electrical Characteristics cont.

$V_{BIAS} (V_S) = 15V$, $T_A = 25^\circ C$ unless otherwise specified. The V_{IN} , and I_{IN} parameters are referenced to GND and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to GND and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Logic "1" input voltage (OUTA=HI, OUTB=HI) (IR4426) Logic "0" input voltage (OUTA=LO, OUTB=LO) (IR4427) Logic "1" input voltage (OUTA=HI), Logic "0" input voltage (OUTB=LO) (IR4428)	—	—	0.8	V	
V_{OH}	High level output voltage, $V_{BIAS}-V_O$	—	—	1.2		$I_o = 0mA$
V_{OL}	Low level output voltage, V_O	—	—	0.1		$I_o = 0mA$
I_{IN+}	Logic "1" input bias current (OUT=HI)	—	5	15	μA	$V_{IN} = 0V$ (IR4426) $V_{IN} = V_S$ (IR4427) $V_{INA} = 0V$ (IR4428) $V_{INB} = V_S$ (IR4428)
I_{IN-}	Logic "0" input bias current (OUT=LO)	—	-10	-30		$V_{IN} = V_S$ (IR4426) $V_{IN} = 0V$ (IR4427) $V_{INA} = V_S$ (IR4428) $V_{INB} = 0V$ (IR4428)
I_{QS}	Quiescent V_S supply current	—	100	200		$V_{IN} = 0V$ or V_S
I_{O+}	Output high short circuit pulsed current	1.5	2.3	—	A	$V_O = 0V$, $V_{IN} = 0$ (IR4426) $V_O = 0V$, $V_{IN} = V_S$ (IR4427) $V_O = 0V$, $V_{INA} = 0$ (IR4428) $V_O = 0V$, $V_{INB} = V_S$ (IR4428) $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	1.5	3.3	—		$V_O = 15V$, $V_{IN} = V_S$ (IR4426) $V_O = 15V$, $V_{IN} = 0$ (IR4427) $V_O = 15V$, $V_{INA} = V_S$ (IR4428) $V_O = 15V$, $V_{INB} = 0$ (IR4428) $PW \leq 10 \mu s$

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AC Electrical Characteristics

$V_{BIAS} (V_S) = 15V$, $C_L = 1000pF$, $T_A = 25^\circ C$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
t_{d1}	Turn-on propagation delay	—	85	160	ns	figure 4
t_{d2}	Turn-off propagation delay	—	65	150		
t_r	Turn-on rise time	—	15	35		
t_f	Turn-off fall time	—	10	25		

Functional Block Diagram IR4426



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Functional Block Diagram IR4427



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Functional Block Diagram IR4428



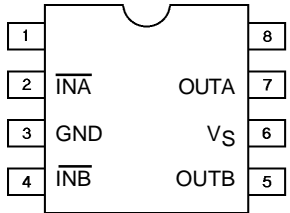
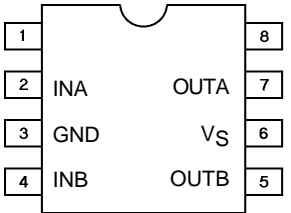
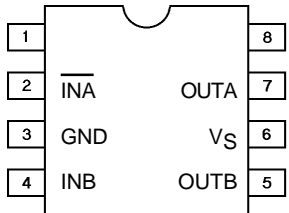
Lead Definitions

Symbol	Description
V_s	Supply voltage
GND	Ground
INA	Logic input for gate driver output (OUTA), out of phase (IR4426, IR4428), in phase (IR4427)
INB	Logic input for gate driver output (OUTB), out of phase (IR4426), in phase (IR4427, IR4428)
OUTA	Gate drive output A
OUTB	Gate drive output B

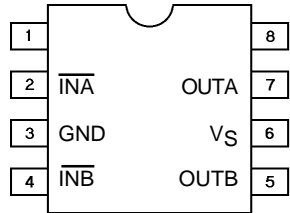
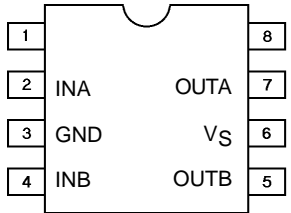
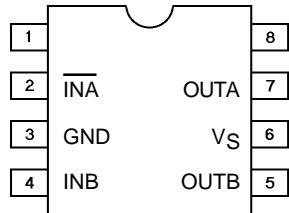
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Lead Assignments

 <p>8 Lead PDIP</p>	 <p>8 Lead PDIP</p>	 <p>8 Lead PDIP</p>
IR4426	IR4427	IR4428
Part Number		

Lead Assignments

 <p>8 Lead SOIC</p>	 <p>8 Lead SOIC</p>	 <p>8 Lead SOIC</p>
IR4426S	IR4427S	IR4428S
Part Number		

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Figure 3. Timing Diagram



Figure 4. Switching Time Waveforms

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Figure 5. Switching Time Test Circuits

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Caseoutline



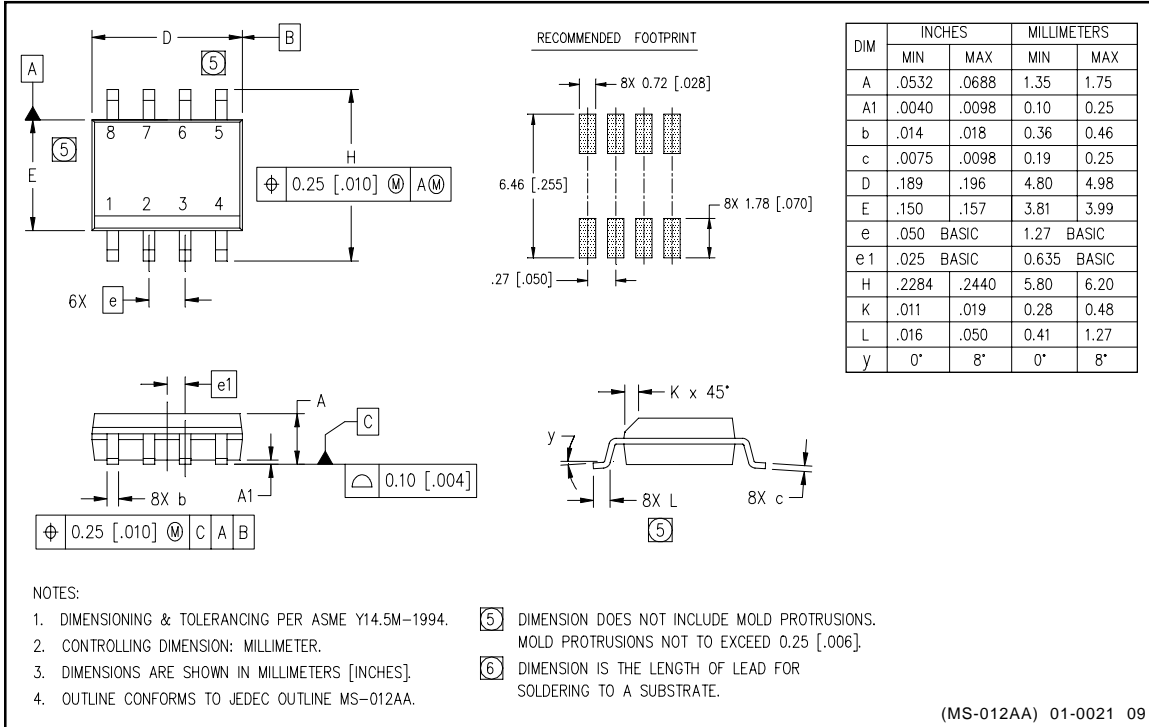
Tape & Reel



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Case Outline - 8 Lead SOIC



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LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR4426 order IR4426
8-Lead SOIC IR4426S order IR4426S
8-Lead PDIP IR4427 order IR4427
8-Lead SOIC IR4427S order IR4427S
8-Lead PDIP IR4428 order IR4428
8-Lead SOIC IR4428S order IR4428S

Leadfree Part

8-Lead PDIP IR4426 order IR4426PbF
8-Lead SOIC IR4426S order IR4426SPbF
8-Lead PDIP IR4427 order IR4427PbF
8-Lead SOIC IR4427S order IR4427SPbF
8-Lead PDIP IR4428 order IR4428PbF
8-Lead SOIC IR4428S order IR4428SPbF

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This product has been qualified per industrial level
Data and specifications subject to change without notice. 3/3/2008